A LOW POWER AND FAST CMOS ARITHMETIC LOGIC UNIT

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ABSTRACT

This thesis presents the design of a low power and fast Complimentary Metal-Oxide-Semiconductor (CMOS) Arithmetic Logic Unit (ALU). ALU is one of the most important parts of a digital computer which is designed to do the arithmetic and logic operations, including bit shifting operation that need to be done for almost any data that is being processed by the central processing unit (CPU). For most applications of all digital circuits, the two important attributes are maximizing speed and minimizing power consumption. The overall performance of the system will depend on the speed of the different modules used in the design. To achieve the desired outcome, the proposed ALU is designed using pass transistor logic (PTL) based multiplexers and 8 transistors (8T) full adder. Tanner EDA V13 with CMOS technology of 0.25µm is used to design and analyze the circuit. Less number of transistors used will result in small design space area thus reducing the power consumption. The result is being analyzed by different values of supply voltage applied to the circuit which ranging from 5V to 1V. The results obtained shows that the minimum power consumption is for V_{dd} equal to 1V with 0.533µW. The speed of the circuit is being measured through the propagation delay of the ALU. The result shows the propagation delay for 1V power supply is 3.65µs.

ABSTRAK

Tesis ini membentangkan reka bentuk Unit Aritmetik Logik (ALU) CMOS yang rendah kuasa dan pantas. ALU adalah salah satu bahagian yang penting dalam komputer digital yang direka untuk melakukan aritmetik dan logik operasi, termasuk operasi anjakan unit yang perlu dilakukan untuk hampir semua data yang sedang diproses oleh unit pemprosesan pusat (CPU). Bagi kebanyakan aplikasi litar digital, terdapat dua ciri-ciri penting iaitu memaksimumkan kelajuan dan mengurangkan penggunaan kuasa. Prestasi keseluruhan sistem akan bergantung kepada kelajuan modul yang berbeza yang digunakan dalam reka bentuk. Untuk mencapai hasil yang dikehendaki, ALU yang direka menggunakan pemultipleks berasaskan *pass transistor logic* (PTL) dan penambah penuh lapan transistor. Tanner EDA V13 dengan menggunakan teknologi CMOS 0.25µm digunakan untuk mereka bentuk dan menganalisis litar ini. Jumlah transistor yang sedikit yang digunakan akan menghasilkan ruang reka bentuk yang kecil dan seterusnya mengurangkan penggunaan kuasa. Keputusan dianalisis dari nilai bekalan voltan yang berbeza yang dibekalkan kepada litar yang terdiri dari 5V ke 1V. Keputusan yang diperolehi menunjukkan penggunaan kuasa paling minimum adalah semasa V_{dd} 1V iaitu sebanyak 0.533µW. Kelajuan litar ALU pula diukur melalui lengah perambatan. Keputusan menunjukkan lengah perambatan paling pendek adalah 3.65µs untuk bekalan kuasa 1V.

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ALU	-	Arithmetic Logic Unit
CPU	-	Central Processing Unit
CMOS	-	Complimentary Metal-Oxide-Semiconductor
V_{dd}	-	Supply voltage
FA	-	Full Adder
Mux	-	Multiplexer
T	-	Transistor
GPU	-	Graphics Processing Unit
FPU	-	Floating-Point Unit
VLSI	-	Very Large Scale Integration
V_{th}	-	Threshold Voltage
PDP	-	Power Delay Product
P_{avg}	-	Average power
W/L	-	Width/Length
FSL	-	Feedback-Switch Logic
DSP	-	Digital Signal Processor
QDI	-	Quasi-Delay-Insensitive
SLTI	-	Static Logic Transistor-level Implementation
PCHB	-	Pre-Charged Half-Buffer
FFT	-	Fast Fourier Transform
C_{in}	-	Carry In

C_{out}	-	Carry Out
CPL	-	Complementary Pass Transistor Logic
BGFSB	-	Back-gate Forward Substrate Bias
t_{pd}	-	Propagation delay
t_r	-	Rise time
t_f	-	Fall time

CHAPTER 1

A LOW POWER AND FAST CMOS ARITHMETIC LOGIC UNIT

1.1 Project Background

One of the important parts of a digital computer is an arithmetic logic unit (ALU). ALU is designed to do the arithmetic and logic operations, including bit shifting operations which are the basic processes that need to be done for almost any data that is being processed by central processing unit (CPU). For most applications of all digital circuits, the two important attributes are maximizing speed and minimizing power consumption. The overall performance of the system will depend on the speed of the different modules used in the design.

CPU can be more powerful, but it also can consume more energy and creates more heat depending on how the ALU is designed. Therefore, it is important to balance between how powerful and complex the ALU is and how expensive the whole unit becomes. Faster CPUs are normally more expensive, consume more power and dissipate more heat.

There are many different power reducing techniques being used to design low power, high-performance chips based on complementary metal-oxide-semiconductor (CMOS) such as reducing voltage, load capacitance or switching frequency of the output node [1]. The most common and effective way of reducing the power consumption is by reducing the supply voltage (V_{dd}) which results in quadratic improvement in the power dissipation of a CMOS circuit [2].

1.2 Problem Statement

As a fundamental part of the microprocessors, ALU performs computing operations and it is typically on the critical path. Therefore, the achievable operating frequency of the whole microprocessor is determined by the operating speed of ALU. At the same time, ALU is also one of the most active components in microprocessor, raising the power and thermal issues. Therefore, the lowest voltage supply to the circuit is needed to reduce power and reducing the propagation delay is required to enhance the speed of the ALU.

1.3 Objectives

For this project, the objectives are:

i. To design a low power ALU

ii. To design a fast ALU

1.4 Scope of Project

All the works on this project were done by using Tanner EDA software with 0.25µm technology. The proposed ALU is limit to 4-bit and it is consisted of full adder (FA) and multiplexer (mux) of 4:1 mux and 2:1 mux. To reduce power consumption and optimize the design space area, less number of transistors was used for the pass-transistor logic based multiplexers of 2:1 and 4:1, and FA of eight transistors (8T).

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter describes the necessary study to design a low power and fast ALU circuit. The first part of this chapter explained about the function of ALU, the operations that it performs, and the types of structure to implement FA in ALU. The second part of this chapter reviewed the technology developments that associated to the proposed design. The last part of this chapter described about the software development used to design and simulate the proposed circuit which is Tanner EDA tool.

2.2 Arithmetic Logic Unit (ALU)

An ALU is an integrated circuit within a CPU or graphics processing unit (GPU) that performs arithmetic and logic operations. Arithmetic operations include addition, subtraction, and shifting operations, while logic operations include Boolean comparisons, such as AND, OR, XOR, and NOT operations. All these operations are in the final processing performed by the processor. After the information has been processed by the ALU, it is sent to the computer memory.

ALUs are designed to perform integer calculations. Therefore, besides adding and subtracting numbers, ALUs often handle the multiplication of two integers, since the result is also an integer. However, ALUs typically do not perform division

operations, since the result may be a fraction, or a "floating point" number. Instead, division operations are usually handled by the floating-point unit (FPU), which also performs other non-integer calculations.

While the ALU is a fundamental component of all processors, the design and function of an ALU may vary between different processor models. For example, some ALUs only perform integer calculations, while others are designed to handle floating point operations as well. Some processors contain a single ALU, while others include several ALUs that work together to perform calculations. Regardless of the way an ALU is designed, its primary job is to handle integer operations. Therefore, a computer's integer performance is tied directly to the processing speed of the ALU.

Most of the digital systems used for very large scale integration (VLSI) applications, extensively use arithmetic operations. Thus, addition has become a fundamental arithmetic operation performed by any ALU, the design and implementation of a 1-bit FA circuit has become the most crucial issue [3]. There are two types of logic structures to implement the FA cell, namely static style and dynamic style. The static FAs are normally simpler, more reliable, and lower power compared to dynamic. However, dynamic FAs are faster and sometimes more compact than static FAs but the drawback of dynamic is it suffers from charge sharing high power due to high switching activity, clock load and complexity [4].

2.3 Technology Development

Study on the technology development is important to ensure a continuous improvement can be made in the specific area. Based on previous studies, [4] can be used to propose a low power and fast ALU. The study from [5], it can be used as a reference in term of ratios of the transistors size used in the FA.

2.3.1 Design of Low Power ALU using 8T FA and PTL Based Mux Circuits [4]

In this paper they proposed an ALU using novel 8T FA and pass transistor logic based multiplexers. A 4:l mux and a 2:l mux were used to design an ALU. FA is an essential component for designing all types of processors like digital signal

processors (DSP), microprocessors, etc. In existing method, FA and multiplexers were designed using transmission gate logic. To reduce the number of transistors, multiplexers were designed using pass transistor logic while FA is designed using 8 transistors logic in the implementation of ALU. The power and the area were greatly reduces to more than 70% compared to the existing method.

2.3.2 A Review Paper on 3T XOR cells and 8T Adder Design in Cadence 180nm [5]

This paper gives a review of already existing 3T XOR cells and provides an optimized value of width/length (W/L) on the basis simulation results obtained which helped to improve the driving capability as to improve the threshold loss problems present in the existing designs of 3T XOR cells. However, the driving capability obtained is not sufficient for large circuits like multipliers. From their best improved version of 3T XOR cell obtained, they designed a FA circuit. They implement all the basic circuits and their improved versions in Cadence Virtuoso for 180nm technology and 1.8V source.

2.3.3 Design of Low Power High Speed ALU Using Feedback Switch Logic [6]

A new dynamic like static circuit family called Feedback-Switch Logic (FSL) has been proposed in this paper. The FSL is suitable for high speed and low power because it offers fast switching, reduced capacitance and input-switching dependent activity factor without the need of clock connection. This paper presents the design of low power high speed 32-bit ALU based on static CMOS and FSL logics at 90nm CMOS process in CADENCE design tool. Simulation results shows that the design of ALU using FSL achieves 14% reduction in delay but at the cost of 8% increased power consumption compared to static CMOS logic. This ALU combines adder, shifter and logical units which are having low power consumption, less delay and uses lesser area. ALU using FSL attained low power and high speed by optimal sizing of transistors.

2.3.4 Low Power Sub-Threshold Asynchronous QDI Static Logic Transistor-Level Implementation (SLTI) 32-bit ALU [7]

In [7], they proposed an asynchronous-logic Quasi-Delay-Insensitive (QDI) static logic transistor-level implementation (SLTI) approach for low power sub-threshold operation. The approach is implemented to design 32-bit pipelined ALUs, the primary computation core for microprocessors, and benchmarked against the reported Pre-Charged Half-Buffer (PCHB). There are two key attributes in this proposed design. First, the proposed SLTI ALU design can perform dynamic voltage scaling seamless by only changing the V_{dd} from nominal (1V) to sub threshold (~0.2V) regions for high speed/low power operation. Second, the ALU achieves ultra-low power dissipation (3.5μW) at the lowest V_{dd} point (~0.15V). For fair of comparison, both implemented ALUs have identical functionality and functional blocks, are implemented using the same 65nm CMOS process. Based on the simulations, the minimum energy point occurs at V_{dd} of 0.2V for SLTI-based ALU and at V_{dd} of 0.3V for PCHB based ALU. The SLTI-based ALU have ~93% and ~89% lower energy on the arithmetic and logic operations respectively from V_{dd} of 1V to V_{dd} of 0.2V. At V_{dd} of 0.2V, with 9 MHz input switching rate, the asynchronous ALU based on their proposed SLTI approach dissipates ~51% and ~44% lower power than the reported PCHB counterpart on the arithmetic and logic operations respectively.

2.3.5 Design of a Low Power, Sub-Threshold, Asynchronous ALU Using a Bidirectional Adder [8]

A novel asynchronous bidirectional ALU is introduced in this paper. The adder in the proposed design is a ripple carry adder with the bidirectional characteristic. The ALU is designed with asynchronous dual rail circuit style. Several ALUs with sizes ranging from 4 bits to 32 bits were built. Their power and performance metrics were compared with the conventional ALUs built with the fast adders designed with dynamic logic style. Significant power reduction with the sub-threshold operating voltage is achieved. Also the design is compared with the ALU design proposed for reversible quantum computers in the CMOS context to show the logic efficiency of

the proposed design around 30 % in area. Power reduction of 9 - 26% was achieved for the addition operation and 19.5 - 75.1% for the logical operation on the proposed 32 bit ALU, compared to the conventional dynamic logic based ALU operated over the voltage range 0.2-0.3V.

2.3.6 Energy – Efficient, High Performance Circuits for Arithmetic Units [9]

This paper present a new full adder structure based on complementary pass transistor logic (CPL) which is faster and more energy efficient than the existing structures. They also proposed a new technique of implementing multiplier circuit using decomposition logic which improves speed and reduces power consumption by reducing the spurious transition on international nodes. There is substantial improvement in the performance of the multiplier structure with the combination of the new adder structure and the decomposition logic. The proposed circuits were implemented using TSPICE for simulation in TSMC 180nm technology.

2.3.7 A Low Power 10-transistor Full Adder Cell for Embedded Architecture [10]

This paper has proposed a full adder cell using 10T which has the advantage of low power consumption and high operating speed. It occupied a small area due to the small transistor count. The objective of low power is achieved at the circuit level by reducing the number of internal node capacitances by eliminating direct paths between the supply voltage and the ground, by maintaining low switching activity in the circuit. The proposed cell is compared with standard transmission gate adder cell and a 16T adder cell and characterized by its low power consumption compared to other adder cells. Using the proposed adder cell, one 4-bit multiplier is constructed and used as a test vehicle to check the performance of the new proposed design in embedded architecture. The circuit is developed using 0.35µm CMOS technology using Cadence development tools and simulated using HSPICE. The circuit consumed 75.2µW at a frequency of 500 MHz.

2.3.8 An Implementation of 1-bit Low Power Full Adder Based on Multiplexer and Pass Transistor Logic [11]

This paper presents the design of low power full adder based on XOR pass transistor logic and transmission gate for carry. They have not connected power supply rail directly, instead of that inputs are given directly to reduce the transition activity and charge recycling capability and this result in great amount of reduction in power consumption. The proposed 14T full adder has been developed using Tanner SPICE simulation. Based on their result, there is saving of power supply by the factor of 30% as compared to 10T full adder and a reduction in power by 26% as compared to the conventional 28T CMOS adder.

2.3.9 A Fast ALU Design in CMOS for Low Voltage Operation [12]

In this paper, a high-speed 4-bit ALU has been designed for 1V operation to demonstrate the usefulness of the back-gate forward substrate bias (BGFSB) method in 1.2μm n-well CMOS technology. The 4-bit ALU employs a ripple carry adder and is capable of performing eight operations which are four arithmetic and four logical operations. The BGFSB has been limited to |0.4|V. The delay time measurements are taken for all operations from the SPICE simulations with and without the back-gate forward substrate bias.

2.4 Software Development

The circuit design of the ALU which consist of FAs and multiplexers for this project was developed by using Tanner EDA tool version 13.0. This integrated front-end tool suite includes S-edit for schematic capture, T-Spice for circuit simulation and W-Edit for waveform viewing and analysis.

2.4.1 T-Spice: Analog Simulation

T-Spice is a complete design capture and simulation solution that provides accuracy and convergence with market-proven reliability. It transforms designer's idea into design and able to quickly simulate large circuit and with a high degree of accuracy. It also offers integration with other design tools and is compatible with industry standard.

2.4.2 S-Edit: Schematic Capture

S-Edit gives the power to handle most complex full custom IC design capture with its tightly integrated with Tanner EDA's T-Spice simulation, L-Edit layout editor, and HiPer verification tools. S-Edit integrates easily with third-party tools and legacy data with its efficient design capture process. S-Edit allows designer to explore design choices and provides an easy-to-use view into the consequences of those choices.

- Operating point result can be viewed directly on the schematic with the S-Edit's tight integration with SPICE simulation which it also allows performing waveform cross-probing to view node voltages and device terminal currents or charges.
- S-Edit imports schematics via Open Access and via EDIF from Cadence, ORCAD and ViewDraw with automatic conversion of schematics and properties for seamless integration of legacy data.
- S-Edit's schematic design checks permits designers to check their design for common errors such as undriven nets, unconnected pins and nets driven by multiple outputs so designers can detect errors early before they running simulations. Figure 2.1 shows an example of the S-Edit window.

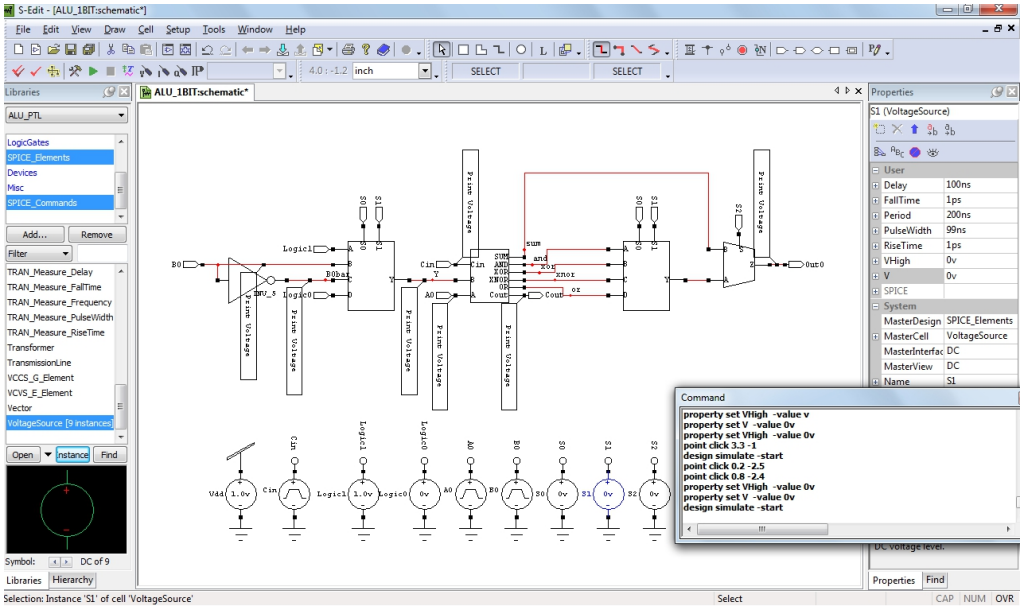

Figure 2.1: S-Edit

2.4.3 W-Edit: Waveform Viewing & Analysis

The W-Edit waveform analysis tool is a comprehensive viewer for displaying, comparing, and analyzing simulation results. W-Edit provides an intuitive multiple-window, multiple-chart interface for easy viewing of waveforms and data in highly configurable formats

- W-Edit is dynamically associated to T-Spice and S-Edit with a run-time update feature which displays simulation results as they are being generated and it also allows waveform cross-probing directly in the schematic editor for faster design cycles.
- W-Edit offers advanced features such as automatically calculating and displaying Fast Fourier Transform (FFT) results in a variety of formats, including dB or linear magnitude, wrapped or unwrapped phase, and real or imaginary parts.
- For advanced analysis and easy comparison with measured data, W-Edit allows creation of new traces based on mathematical expressions of other traces. Figure 2.2 shows an example of W-Edit window.

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